Anatomy of a Forward-Looking Open Standard

Sam Fuller, Motorola Networking and Computing System Group **Tom Cox,** Tundra Semiconductor Corp.

he electronics design field is not for the faint of heart. An intensely competitive industry, product design is the nucleus of a vibrant market focused on new technologies and applications and the next major upgrade. The proprietary details of a company's technology are prized information for most vendors. To manufacturers, R&D is an ongoing investment in the talent and resources that will yield the next gainful product or leap in technology. Struggling against the sheer force of market pressure, companies must bring innovations to fruition faster than the last new increment.

So why would an electronics-based company open its treasure chest and give away sophisticated technology by participating in developing an open standard? Why would battle-tested engineers and product development technologists devote their energy to sharing hard-gained experience with competitors?

In some situations, collaboration can be better for a company than competition. Few products operate in a vacuum, and we must resolve shared interoperability issues in an open environment. Cooperating within the industry to create an open standard can be more effective than embracing proprietary technology. An enterprise that keeps market-making expertise private might slip ahead of its com-



The RapidIO interconnect specification represents the state of the art in standards development.

petitors by exploiting an existing, but limited, consumer demand. But an open standard fuels growth and innovation, and the market expands exponentially, producing more opportunity

and higher sales volumes for all.

Bringing the RapidIO interconnect specification to market as an open standard that incorporates preexisting standards where possible demonstrates state-of-the-art standards development. Using the procedures developed by standards bodies such as the IEEE smoothed the path for converting RapidIO from an open standard managed by a trade association or consortium to one approved by an internationally recognized standards organization.

FROM IMPASSE TO OPPORTUNITY

An industry typically proposes standards when it reaches a technological turning point or an impasse that limits future market development. In our industry, hierarchical and shared buses such as peripheral component interconnect (PCI) have reached their per-

formance limits in terms of supporting the ever-faster semiconductor devices being brought to market. The need for high-speed, reliable connectivity for next-generation system design was the driving force behind developing the RapidIO interconnect architecture.

RapidIO defines a switch-fabric control-plane interconnect developed specifically to achieve high-performance, low-cost, reliable, and scalable system connectivity in embedded, networking, and communications devices. The broadly applicable specification offers built-in error detection, low latency, and a high degree of determinism.

The architecture supports transmission rates up to 64 Gbits per second and offers significantly greater bandwidth, more flexibility, and higher reliability than currently used bus interconnects, yet it works with existing PCI and CPU architectures. Chips from Motorola, IBM, Tundra, and other vendors that use the specification will be compatible. Designing to the standard will eliminate redundant development costs so that manufacturers can bring products to market less expensively. Improved compatibility at the interconnect level can enhance system reliability and performance.

Developed in collaboration with silicon providers and leading equipment vendors worldwide, the RapidIO interconnect architecture addresses shared design issues rather than a specific vendor's proprietary needs. Motorola and Mercury Computer spearheaded the effort, transferring work to the RapidIO Trade Association (RTA), an independent industry body open to all, early in the development process.

More than 40 member companies, including major networking and communications vendors, spent more than a year reviewing and enhancing the specification before ratifying it. The RTA continues to govern the specification, which can be downloaded from the association's Web site (http://www.RapidIO.org).

STATE-OF-THE-ART STANDARD DEVELOPMENT

Acknowledging our predecessors' efforts, the RTA guided and controlled the process based on previously established standard methodologies that ensured an open and equitable environment. Industry experts directed the process to generate a specification suitable to a broad market while meeting the embedded and communications industries' specific needs. Member companies contributed technology or experience in their specialties. The resulting pool of knowledge expanded well beyond the capabilities of any single company seeking to develop its own similar technology.

Leveraging experience

Several RTA member companies also contributed experience to the existing standards that were integrated into the specification. Already widely implemented throughout the industry, these supporting standards will reduce development time and costs for companies adopting RapidIO and enhance the final product's overall quality. For example, we benefited from two decades of experience acquired by several association members while developing the popular IEEE 802 standard for local area networks.

Mercury Computer leveraged its experience developing the ANSI standard RaceWay technology to help generate the RapidIO specification. Company co-founder Robert C. Frisch, who guided development of the Race-Way architecture, participated in the RTA's efforts. Motorola brought its expertise in microprocessors, microprocessor buses, and cache coherent

multiprocessor systems. Xilinx engineers applied their experience in high-speed electrical signaling and programmable logic to RapidIO. EMC engineers, with a history of developing fault tolerant systems, ensured the specification's robust operation.

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The most time-consuming responsibilities fell on the RapidIO Technical Working Group, which participated in weekly conference calls and bimonthly face-to-face meetings to discuss all aspects of the specification. At times, the calls generated heated debates, but the process continued to move forward with balloting and majority rule.

To ensure participation and contribution, companies were required to participate in the calls and meetings to have the right to vote on specification details. Competitive issues generally fell by the wayside as engineers brought invaluable expertise to the table. No single vendor unduly influenced the specification to its own advantage.

Two computer veterans with ties to the Internet's founding, Louis-François Pau of Ericsson and Gary Robinson of EMC, have been involved in developing many of the standards now commonly accepted as part of the industry infrastructure. Pau has been an important advocate for RapidIO in the wireless industry and has helped guide the development process. Robinson is preparing the specification for submission to recognized international standards organizations such as the IEEE and ISO.

Vendor contributions

In addition to senior-level design engineers from member companies, industry veterans directed the specification development process based on their experience in the standards world. Dan Bouvier, PowerPC architecture manager at Motorola, was involved in the early stages of the PCI standards development effort. As chair of the RapidIO Technical Working Group, he enforced the open methodology that ensured fair discussion of the specification. Bryan Marietta, also from Motorola, served as the specification editor and worked with Bouvier to apply the standardized OSI layer model to the technology.

he software-transparent RapidIO interconnect specification resolves an essential design bottleneck while also creating a clear migration path for systems based on existing or legacy architectures. The process of bringing this specification to market demonstrates that contributing to a collaborative standards development effort can be beneficial to all the participants. Designing to the specification can reduce manufacturing costs and time to market while significantly increasing bandwidth.

Sam Fuller, chair of the RapidIO Trade Association, is the director of engineering at the Motorola Networking and Computing System Group. Contact him at Sam.Fuller@motorola.com

Tom Cox, chair of the RapidIO Marketing Working Group, is the director of strategic planning at Tundra Semiconductor Corp. Contact him at tom. cox@tundra.com.

Editor: Gary S. Robinson, EMC, 228 South Street, Hopkinton, MA 01748-9103; robinson_gary@emc.com